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 October 1987 ASPLOS-II: Proceedings of the second international conference on  
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 T. A. Cargill, B. N. Locanthi  
October 1987 ACM SIGOPS Operating Systems Review, Volume 21 Issue 4  
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5 [Process cruise control: event-driven clock scaling for dynamic power management](#)

 Andreas Weissel, Frank Bellosa  
October 2002 CASES '02: Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems  
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Scalability of the core frequency is a common feature of low-power processor architectures. Many heuristics for frequency scaling were proposed in the past to find the best trade-off between energy efficiency and computational performance. With complex ...

Keywords: clock scaling, event counters, power management, scheduling

6 [Rapid profiling via stratified sampling](#)


 S. Subramanya Sastry, Rastislav Bodík, James E. Smith  
May 2001 ACM SIGARCH Computer Architecture News, Volume 29 Issue 2  
Publisher: ACM

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*Sophisticated binary translators and dynamic optimizers demand a program profiler with low overhead, high accuracy, and the ability to collect a variety of profile types. A profiling scheme that achieves these goals is proposed. Conceptually, the ...*

7 [The benefits of event-driven energy accounting in power-sensitive systems](#)

 Frank Bellosa  
September 2000 EW 9: Proceedings of the 9th workshop on ACM SIGOPS European workshop: beyond the PC: new challenges for the operating system  
Publisher: ACM

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A prerequisite of energy-aware scheduling is precise knowledge of any activity inside the computer system. Embedded hardware monitors (e.g., processor performance counters) have proved to offer valuable information in the field of performance analysis. ...



Rapid profiling via stratified sampling

S. Subramanya Sastry, Rastislav Bodik, James E. Smith

June 2001 I SCA '01: Proceedings of the 28th annual international symposium on Computer architecture

Publisher: ACM

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*Sophisticated binary translators and dynamic optimizers demand a program profiler with low overhead, high accuracy, and the ability to collect a variety of profile types. A profiling scheme that achieves these goals is proposed. Conceptually, the ...*

9 Enhancements for hyper-threading technology in the operating system: seeking the optimal scheduling

Jun Nakajima, Venkatesh Pallipadi

December 2002 W I ESS'02: Proceedings of the 2nd conference on Industrial Experiences with Systems Software - Volume 2, Volume 2

Publisher: USENIX Association

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Hyper-Threading Technology (HT) is Intel®'s implementation of Simultaneous Multi-Threading (SMT). HT delivers two logical processors that can execute different tasks simultaneously using shared hardware resources on the processor package. In general ...

10 Data Centric Cache Measurement on the Intel Itanium 2 Processor

Bryan R. Buck, Jeffrey K. Hollingsworth

November 2004 SC '04: Proceedings of the 2004 ACM/IEEE conference on Supercomputing

Publisher: IEEE Computer Society

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Processor speed continues to increase faster than the speed of access to main memory, making effective use of memory caches more important. Information about an application's interaction with the cache is therefore critical to performance tuning. To ...

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